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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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EXAMINER

PAPE, ZACHARY

| | |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

2835

DATE MAILED: 08/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/824,223

Applicant(s)

LIN ET AL.

Examiner

Zachary M. Pape

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. **Therefore, the fan of claims 12 and 27** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-11, 13-26, 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamori (US 5,995,370) in view of Frank (US 4,991,002).

With respect to claim 1, Nakamori teaches a function module comprising: a first circuit board (7) including a first surface (See present office action Fig 1 below) with a first ground layer (9) formed thereon; a second circuit board (13) coupled to the first circuit board (Via 16), including a second surface (See present office action Fig 1 below) facing the first surface, wherein a second ground layer (3) is formed on the second surface. Nakamori fails to teach a plate-type heat dissipation device, disposed between the first circuit board and the second circuit board, abutting the first ground layer and the second ground layer respectively.

Frank teaches a function module comprising a heat dissipation device (90) disposed between first and second layers of semiconductors (100, 100' as illustrated in Fig 9) abutting first and second grounding layers respectively. It would have been obvious to one of ordinary skill in the cooling art at the time the invention was made to combine the heat dissipation device (90) of Frank with the function module of Nakamori to provide enhanced cooling to the circuit boards (Frank, Column 3, Lines 40-48).

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combine the heat dissipation device (90) of Frank with the function module of Nakamori to provide enhanced cooling to the circuit boards (Frank, Column 3, Lines 40-48).

With respect to claim 16, Nakamori further teaches that the first heat conduction layer is a ground layer of the first circuit board, and the second heat conduction layer is a ground layer of the second circuit board (Nakamori; Column 3, Lines 17-20 & 28-31).

With respect to claims 2 and 17, Nakamori further teaches that the first circuit board further includes a third surface (See present office action Fig 1 above), opposite the first surface, with a first device (1) located thereon.

With respect to claims 3 and 18, Nakamori further teaches that the second circuit board (13) further includes a fourth surface (See present office action Fig 1 above) opposite to the second surface, with a second device (6) located thereon.

With respect to claims 4, 5, 19, and 20 Nakamori further teaches that the first and second ground layers (3, 9) comprises a copper layer (Column 3, Lines 28-31).

With respect to claims 6 and 21, Nakamori further teaches a flat cable (16) connecting the first circuit board and the second circuit board, providing communicability therebetween (Column 5, Lines 4-14 with emphasis on lines 12-14).

With respect to claims 7 and 22, Nakamori further teaches that the first circuit board (7) includes a first connector (See present office action Fig 1 above), the second circuit board (13) includes a second connector (See present office action Fig 1 above) corresponding to the first connector, and the first circuit board and the second circuit board communicate with each other by the respective connectors.

With respect to claims 8 and 23, Nakamori further teaches that the first connector is located on the first surface, and the second connector is located on the second surface (As illustrated in Fig 1 above the connectors are located on the first and second surfaces for at least the reason that they touch each surface).

With respect to claims 9 and 24, Nakamori further teaches a slot connector (16, wherein the above mentioned connectors are the slots) connecting the first circuit board (7) and the second circuit board (13), providing communicability therebetween.

With respect to claims 10 and 25, Frank further teaches that the plate-type heat dissipation device is a plate-type heat pipe, a copper plate, a plate-type copper block, a micro fin (Frank, Fig 9), a water-cooling device, or a vapor chamber.

With respect to claims 11 and 26, Frank further teaches a heat dissipation fin (98), connected to the plate-type heat dissipation device, for further dissipation of heat therefrom (Frank, Fig 9).

With respect to claims 13 and 28, Nakamori further teaches the use of a paste (12) layer used to connect elements together and further aide in emitting out the heat radiation from the CPU and other components on the circuit boards (Nakamori; Column 3, Lines 36-50) and therefore it is an obvious modification of the teachings of Nakamori to use the paste as first and second adhesion layers between the heat dissipation device and the heat conducting layers.

With respect to claims 14 and 29, Nakamori further teaches that both the first adhesion layer and the second adhesion layer comprise one selected from group



Frank teaches a function module comprising a heat dissipation device (90) disposed between first and second layers of semiconductors (100, 100' as illustrated in Fig 9) abutting first and second grounding layers respectively. It would have been obvious to one of ordinary skill in the cooling art at the time the invention was made to

consisting of brazing solder, solder, thermal interface material (Nakamori, Column 3, Lines 36-50), grease and the combination thereof respectively.

3. Claims 12 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamori in view of Frank and further in view of DeHoff et al. (US 6,408,935).

With respect to claims 12 and 27, Nakamori in view of Frank teaches the limitations of claim 11 above, but fails to teach that the function module further comprises a fan connected to the heat dissipation fin for further dissipation of heat therefrom. De Hoff et al. teaches the conventionality of attaching a fan (25) to a heat dissipation fin (23). It would have been obvious to one of ordinary skill in the cooling art at the time the invention was made to combine the fan of DeHoff et al. with the function modules of Nakamori and Frank to provide enhanced cooling to the fins (DeHoff; Column 3, Lines 40-43). Enhancing the cooling of the fins reduces the heat buildup on the devices thus reducing malfunctions and breakdowns.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Donahoe et al. (US 5,808,869); Duesman et al. (US 6,201,695) further teach heat dissipating devices cooling circuit boards.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zachary M. Pape whose telephone number is 571-272-

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2201. The examiner can normally be reached on Mon. - Thur. & every other Fri.
(8:00am - 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn Feild can be reached at 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ZMP

BORIS CHERVINSKY
PRIMARY EXAMINER

Boris I. Chervinsky
8/24/05